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10/602,020	06/24/2003	Frederic Reblewski	003921.00135	7641

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EXAMINER	
SAXENA, AKASH	

ART UNIT	PAPER NUMBER
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/602,020	REBLEWSKI ET AL.	
	Examiner	Art Unit	
	AKASH SAXENA	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 August 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 16-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 16-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claim(s) 1-2 and 16-31 has/have been presented for examination based on amendment filed on 10/26/2009.
2. Claim(s) 1, 2, 16-20, 23, 26 and 29-31 is/are amended.
3. Claim(s) 3-15 and 32 are cancelled.
4. Claim(s) 1-2 and 16-28 are rejected under 35 USC § 103 by combination of Swoboda, Litt and Tausheck as previously.
5. Claims 29-31 are newly rejected under 35 U.S.C. 103(a) as being unpatentable over Litt, in view of Swoboda, further in view of Swoboda2.
6. This action is made FINAL. The examiner's response is as follows.

Claim Objection

7. Specifically the current amendment to claims is non-compliant as claims 23 & 25 are amended however the status states (originia) and (Previously Presented) respectively.

Response to claim rejection under 25 USC 112

8. Examiner has withdrawn the rejection under this statue due to amendment of claims 1, 2 and 16-19.

Response to Arguments for Claim Rejections - 35 USC § 103

(Argument 1) Applicant has argued in Remarks Pg.11-12:

> ...Claim 1 does not have anything equivalent to the data compression map of Swoboda. Removal of data compression map from Swoboda renders Swoboda unsatisfactory for its intended purpose of compressing state data for transmission while preserving the entire state data. Swoboda is different from and does not render obvious Claim 1 for at least above highlighted reason....

(Response 1) In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "methodology of identifying the data of interest" E.g. as data compression technique in Swoboda) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Applicant agrees that the "data compression map" is taught by Swoboda. Swoboda compresses the size of trace state data, akin to instant invention, however applicant has not claimed how the data of interest from state data is identified (unlike Swoboda). Unless a specific methodology for selecting data of interest is claimed which reads over Swoboda's data of interest, Swoboda reads over instant invention and applicant's arguments are found to be unpersuasive.

(Argument 2) Applicant has argued in Remarks Pg.13-15:

> Regarding Independent claims 29-31

(Response 2) Applicant's arguments with respect to claim 29-31 have been considered but are moot in view of the new ground(s) of rejection. The new limitation is taught by Swoboda 2.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 1-2, 16-28 rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Publication No. 2002/0065642 A1 by Gary L. Swoboda (Swoboda hereafter), in view of U.S. Patent No. 6,816,989 issued to Timothe Litt (Litt hereafter), further in view of US Patent No. 6092127 issued to Eric G. Tausheck (Tausheck hereafter).

Regarding Claim 1

Swoboda teaches a method in an emulation system (Swoboda: Fig.2 & associated disclosure), comprising receiving a first sample of state data (Swoboda: Fig.9 & and associated disclosure), the first sample of state data having a plurality of bits and being descriptive of one or more states in an emulation system (Swoboda: Fig. 9 & associated disclosure; Fig.2-4 [0007][0066]); identifying a first data of interest in the first sample of state data (Swoboda: Fig.9 state data having at least Data, Address, PC"), wherein the data of interest is a subset of the plurality of bits of first sample of state data (Swoboda: Fig.19 & [0121]).

Swoboda teaches identifying first ignored data in the first sample of state data (Swoboda: Fig.19 & [0121]] – as Byte 0, 3, 4, 6, and 7 as ignored data), the first ignored data being a subset of the bits of the first sample of state data (all the bytes in the Fig.19) and different from the first data of interest (In Fig.19 bytes sent 1, 2 and 5).

Although Swoboda is concerned with storage of trace information, through compression (Swoboda: [0117]-[0118]) it does not explicitly teach determining residual storage of trace buffer and selecting the next buffer if the first buffer is full.

Litt teaches determining if residual storage space in a first buffer exists as smart buffers, which are aware of the buffer state (full or available) of each location in the smart buffer (Litt: Col.10 Lines 12-46). Litt also teaches receiving a first sample of state data (Litt: Col.8 Lines 33-48), sorting the first sample (Litt: Col.7 Lines 20-67), and storing the sorted first sample of state data in the smart buffer (Litt: Fig.2).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Litt to Swoboda as Litt & Swoboda are primary concerned with offloading the trace information. The motivation to combine would be that Litt provides arbitration logic to unload multiple trace buffer (Litt: Fig.2 & associated text) lacking in Swoboda to ease the unloading pressure making the system run faster with appropriate prioritization, especially when trace offloading rates are different from trace generation rate (Swoboda: Fig.22, [0128]-[0129]).

Litt & Swoboda do not explicitly teach if it is determined that residual storage space in the first buffer does not exist, sorting the first data of interest from the first ignored data by storing the first data of interest in a second buffers.

Tausheck teaches if it is determined that residual storage space in the first buffer does not exist, sorting the first data of interest from the first ignored data by storing the first data of interest in a second buffers (Tausheck: Col.2 Lines 38-45).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Tausheck to Litt & Swoboda as Litt & Swoboda are primary concerned with offloading the trace information, however do not disclose handling of multiple offload buffers. The motivation to combine would be that Litt and Swoboda disclose buffer which are FIFO buffer (Litt: Col.10 Lines 13-37; Swoboda: [0128]), however buffer switching is not disclosed by either to ease buffer pressure and overflow condition, which is taught by Tausheck as handing multiple DMA buffers is an analogous situation where switching happens between the full buffers (Tausheck: Abstract).

Regarding Claim 2

Swoboda teaches receiving a second sample of state data (Swoboda: [0094] at least [0121] & Fig 19); identifying second data of interest in the second sample of state data (Swoboda: Fig.9 state data having at least Data, Address, PC", Fig.21 & 24 at least), the second data of interest being a subset of the plurality of bits of the second sample of state data (Swoboda: Fig.19 & [0121]).

Although Swoboda is concerned with storage of trace information, through compression (Swoboda: [0117]-[0118]) it does not explicitly teach *determining if residual storage space in whether the first buffer exists after storing the first data of interest in the first buffer and if it is determined that residual storage space in the first buffer exists, storing at least a portion of the second data of interest in the first buffer after storing the first data of interest in the first buffer, and if it is determined that*

residual storage space in the first buffer does not exist, storing at least a portion of the second data of interest in the second buffer.

Litt teaches teaches *determining if residual storage space in whether the first buffer exists after storing the first data of interest in the first buffer and if it is determined that residual storage space in the first buffer exists, storing at least a portion of the second data of interest in the first buffer after storing the first data of interest in the first buffer* as smart buffers, which are aware of the buffer state (full or available) of each location in the smart buffer (Litt: Col.10 Lines 12-46).

Litt does not explicitly teach if it is determined that residual storage space in the first buffer does not exist, storing at least a portion of the second data of interest in the second buffer.

Tausheck teaches if it is determined that residual storage space in the first buffer does not exist, sorting the first data of interest from the first ignored data by storing the first data of interest in a second buffers (Tausheck: Fig.3, Col.2 Lines 38-45).

Regarding Claim 16

Litt teaches step of identifying information associated with the first data of interest as importance control bit (Litt: Col.9 Line 45 – Col.10 Line 12) and storing sample information to a memory storage location associates with each sample as storing importance control bit (Litt: Col.9 Line 45 – Col.10 Line 12). Applicant has qualified the data as "state data" and subset of that as "data of interest". These qualifications do not alter the methodology and is intended use of the method.

Regarding Claim 17

Litt teaches *information comprises a bit position of the first data of interest within of-the first sample of state data* as storing the importance/control of the sample based on the position/length of the sample header. This counter associated stores the bit position of the ticks (segments of the sample – See Col.6 Lines 49-60) of the sample (Litt: Col.14 Lines 5-23; Col.10 Lines 47-60). Applicant has qualified the data as "state data" and subset of that as "data of interest". These qualifications do not alter the methodology and is intended use of the method.

Regarding Claim 18

Swoboda teaches pin manager and pin macros for identification of output pins where the trace will be outputted (Swoboda: Fig.22; [0128]). Applicant has qualified the data as "state data" and subset of that as "data of interest". These qualifications do not alter the methodology and is intended use of the method.

Regarding Claim 19 (Updated 2/12/09)

Claim 19 repeats the limitations of claims 1 & 16, where the subsequent packets are stored in the memory and is rejected for the same reasons as parent claims. Also see Swoboda Fig.22 and 22A. Applicant has qualified the data as "state data" and subset of that as "data of interest". These qualifications do not alter the methodology and is intended use of the method.

Swoboda teaches the second data of interest includes at least first and second portions separated from each other within the second sample of state data by at least one bit that is not part of the second data of interest (Swoboda: *Fig.19 &*

[0121], See Data Byte 2 and Data Byte 5); the first and second portions of the second data of interest being stored such that they are no longer separated from each other by the at least one bit (See Fig.;18-19 and 24).

Litt teaches identifying information associated with the second data of interest and storing the information to a memory storage location as storing the importance /control of the sample based on the position/length of the sample header. This counter associated stores the bit position of the ticks (segments of the sample – See Col.6 Lines 49-60) of the sample (Litt: Col.14 Lines 5-23; Col.10 Lines 47-60). Plurality of state data and data of interest would be obvious in view of Fig.2 of Swoboda.

Regarding Claim 20 (Updated 2/12/09)

Litt teaches an apparatus having a first select logic device configured to receive samples of state data, to sort samples of state data, and to identify data of interest from each of the samples of state data (Litt: Fig.2, Elements 210 & 215, Col.6 Lines 3-34).

Swoboda teaches wherein selected bit locations of the data of interest from at least two samples are different as it is obvious that not every sample state data layout would look identical to the exemplary sequence presented in Swoboda Fig.19. A different sequence of bytes, other than the one listed in Fig.19, would result in different bytes selected based on rationale presented in [0121]. Therefore Swoboda teaches this limitation.

Further Swoboda teaches the sorting results in a contiguous set of bits of interest (Fig.19 Byte 1 & 2) and a contiguous set of ignored bits (Fig.19 Byte 3 & 4), the continuous set of bits of interest being different from the continuous set of ignored bits (Fig.19). Further, Litt teaches the first select logic device comprises a data of interest sorter (Litt: Fig.2 Packet Prediction and parsing logic with the Prioritization of packets; Col.10 Lines 47-Col.11 Line 6).

Litt teaches first and second buffers coupled to the first select logic device and configured to receive the contiguous set of bits of interest (Litt: Fig.2 Elements 225a 225b, also see Swoboda: Fig.24); a second select logic device coupled to the first and second buffers and configured to select the first and second buffers in an alternating manner to drain the selected buffer (Litt: Fig.2 Elements 250); and an output storage device coupled to the second select logic device and configured to receive data drained from the selected buffer (Litt: Fig.1 Element 50).

Swoboda teaches wherein the filling results in the contiguous set of ignored bits not being preserved by the first select logic device as ignoring the unsent bits (Fig.19 and associated disclosure).

Litt does not teach select data of interest being filled in an alternating manner in each buffer.

Tausheck teaches that trace data is filled in the alternating manner in the trace buffers and then emptied in the alternating manner (Tausheck: Col.5 Lines 62-Col.6 Lines 67 at least).

Regarding Claim 21

Litt teaches first select logic comprises a multiplexer (Litt: Fig.2 Elements 245a & 245b).

Regarding Claim 22

Litt teaches second select logic (as arbitration logic) comprises a multiplexer (Litt: Fig.2 Elements 250; Col.11 Line 56-Col.12 Line 43) where the selection between the buffers to offload the data of interest from them.

Regarding Claim 23

Litt & Tausheck teach first select logic device (Litt: 245a & b) is configured to send contiguous set of bits of interest to second buffer responsive to first buffer becoming full (Tausheck: Col.5 Lines 62-Col.6 Lines 67 at least).

Regarding Claim 24

Litt teaches the first select logic device comprises a data of interest sorter (Litt: Fig.2 Packet Prediction and parsing logic with the Prioritization of packets; Col.10 Lines 47-Col.11 Line 6).

Regarding Claim 25

Claim 25 discloses similar limitations as claim 16 and is rejected for the same reasons as claim 16. Litt teaches step of storing sample information associates with each sample as importance control bit (Litt: Col.9 Line 45 – Col.10 Line 12).

Regarding Claim 26

Claim 26 discloses similar limitations as claim 17 and is rejected for the same reasons as claim 17. Litt teaches storing the importance/control of the sample based

on the position/length of the sample header. This counter associated stores the bit position of the ticks (segments of the sample – See Col.6 Lines 49-60) of the sample (Litt: Col.14 Lines 5-23; Col.10 Lines 47-60).

Regarding Claim 27

Claim 27 discloses similar limitations as claim 18 and is rejected for the same reasons as claim 18.

Regarding Claim 28

Litt teaches output storage device is configured to store information associated with each of the samples of state data as header to each sample that contains sample relevant data (Litt: Col.6 Line 61- Col.7 Line 19).

10. ----- *This page is left blank after this line* -----

11. **Claims 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over, U.S. Patent No. 6,816,989 issued to Timothe Litt (Litt hereafter), in view of U.S. Patent Publication No. 2002/0065642 A1 by Gary L. Swoboda (Swoboda hereafter), further in view of Patent Publication No. 20010034859 A1 by Gary L. Swoboda et al (Swoboda2 hereafter).**

Regarding Claim 29 (Updated 12/31/09)

Litt teaches determining a trace data fill rate of each of a plurality of trace data chains as various trace streams with various rates in the bandwidth manager section (Litt: Col.4 Lines 21-25, 55-65); determining a schedule for associating a plurality of pins with the plurality of trace data chains to transfer data out of the trace data chains based at least upon the determined trace data chain fill rates as decision to offload data by the arbitration manager based on the pressure on the trace buffer once it gets full due to higher fill rate (Litt: Col.12 Lines 8-31).

Litt does not teach a pin manager explicitly that would perform the steps of offloading the data.

Swoboda teaches pin manager and pin macros for identification of output pins where the trace will be outputted (Swoboda: Fig.22; [0128]).

Swoboda teaches one of the plurality of pins is shared by at least two trace data chains as plurality of pins in the trace output ([0017], [0051], [0052], [0058], [0073], [0092], [0094] at least) where there are plurality of trace data chains (See Fig,2, Trace Inputs and Identify information forming trace data chains collected by Trace Collection 21).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Swoboda to Litt to enhances the Litt's teaching by adding a Pin Manager/macro function to arbitration logic and output section of Litt's teaching. To clarify further, The motivation to combine would have been that Swoboda and Litt are concerned with trace data capture where Swoboda and Litt output the trace data to a debugger (Litt: Fig.2; Swoboda: Fig.2, 22, 23, 23A-B) where the pin management is obvious for such data offloading. Swoboda explicitly discloses the pin manager, where the pins for trace & debug can be dynamically allocated reducing the limited pin count pressure in offloading trace information (Swoboda: Fig.22; [0128]).

Swoboda teaches pin manager however is moot on detailed implementation of the pin manager and does not explicitly teach along with Litt, wherein the plurality of pins change from a first clock cycle to a second clock cycle.

Swoboda2 teaches the plurality of pins change from a first clock cycle to a second clock cycle as dynamic configuration of the pins based on various debug jobs and wire list walking (Swoboda2: [0120]-[0132])

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Swoboda2 to Swoboda as both the works are by the same inventor and Swoboda2 provides in depth detailed view of the pin manager mentioned summarily in Swoboda.

Regarding Claim 30 (Updated 2/12/09)

Claim 30 discloses similar limitations as claim 29 and is rejected for the same reasons as claim 29. The bandwidth allotment is determined by the arbitration logic and directions from source clock (Litt: Col.12 Lines 57-Col.13 Line 27). Litt does not explicitly teach the pin schedule selection, which is taught by Swoboda (Swoboda: Col.10 Lines 3-4).

Swoboda teaches one of the plurality of pins is shared by at least two trace data chains as plurality of pins in the trace output ([0017], [0051], [0052], [0058], [0073], [0092], [0094] at least) where there are plurality of trace data chains (See Fig,2, Trace Inputs and Identify information forming trace data chains collected by Trace Collection 21).

Motivation to combine Litt and Swoboda is the same as claim 29 above.

Swoboda teaches pin manager however is moot on detailed implementation of the pin manager and does not explicitly teach along with Litt, wherein the plurality of pins change from a first clock cycle to a second clock cycle.

Swoboda2 teaches the plurality of pins change from a first clock cycle to a second clock cycle as dynamic configuration of the pins based on various debug jobs and wire list walking (Swoboda2: [0120]-[0132])

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Swoboda2 to Swoboda as both the works are by the same inventor and Swoboda2 provides in depth detailed view of the pin manager mentioned summarily in Swoboda.

Regarding Claim 31 (Updated 2/12/09)

Claim 31 discloses similar limitations as claim 30 and is rejected for the same reasons as claim 30. Litt teaches the limitation where the trace chain data fill rates are determined and matched with the data output rate from the arbitration logic. Arbitration logic multiplexer selects the input (pins) from smart buffer based on the fill rate and distress (due to higher fill rate in a smart buffer) (Litt: Col.11 Lines 56-Col.13 Line 37.

Swoboda teaches one of the plurality of pins is shared by at least two trace data chains as plurality of pins in the trace output ([0017], [0051], [0052], [0058], [0073], [0092], [0094] at least) where there are plurality of trace data chains (See Fig,2, Trace Inputs and Identify information forming trace data chains collected by Trace Collection 21).

Motivation to combine Litt and Swoboda is the same as claim 29 above.

Swoboda teaches pin manager however is moot on detailed implementation of the pin manager and does not explicitly teach along with Litt, wherein the plurality of pins change from a first clock cycle to a second clock cycle.

Swoboda2 teaches the plurality of pins change from a first clock cycle to a second clock cycle as dynamic configuration of the pins based on various debug jobs and wire list walking (Swoboda2: [0120]-[0132])

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Swoboda2 to Swoboda as

both the works are by the same inventor and Swoboda2 provides in depth detailed view of the pin manager mentioned summarily in Swoboda.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AKASH SAXENA whose telephone number is (571)272-8351. The examiner can normally be reached on 8:00- 6:00 PM Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Akash Saxena/
Examiner, Art Unit 2128

/Hugh Jones/

Primary Examiner, Art Unit 2128